Xilinx 仿真库编译

1、 ISE 新建工程

点击 New Project



	fions, and comment for the project
Name:	fft_pro
Location:	C:\Users\irene\Desktop\ceshill\fft_pro → 洗择要保存的路径
Working Directory:	C:\Users\irene\Desktop\ceshill\fft_pro
Select the type of Top-level source t	top-level source for the project

```
New Project Wizard
                                                                             ×
+Project Summary
    Project Navigator will create a new project with the following specifications.
 Project:
    Project Name: fft pro
    Project Path: C:\Users\irene\Desktop\ceshill\fft pro
     Working Directory: C:\Users\irene\Desktop\ceshill\fft pro
     Description:
     Top Level Source Type: HDL
 Device:
    Device Family: Spartan6
     Device:
               xc6slx4
     Package:
                   tqg144
     Speed:
                  -3
     Top-Level Source Type: HDL
     Synthesis Tool: XST (VHDL/Verilog)
     Simulator: Modelsim-SE Verilog
    Preferred Language: Verilog
     Property Specification in Project File: Store all values
     Manual Compile Order: false
     VHDL Source Analysis Standard: VHDL-93
     Message Filtering: disabled
 More Info
                                                 < Back
                                                            Finish
                                                                       Cancel
```

点击 Finish, 完成新建工程。

2、 Xilinx 仿真库编译

开始-》所有程序-》xilinx design tools-》simulation library compilation wizard。路径可能不同,只要找到 simulation library compilation wizard 并打开即可。



打开后选择相关的配置项: select simulator 选择 modelsim SE; 我的电脑是 32 位,所以选择 32 位; simulator executable location 中填入 modelsim 所在 的路径,即安装目录下可执行文件 modelsim.exe 所在的路径,其它不用做修改, 点击 next。

Na Xilinx Simulation Library Compilation Wizard - Select Simulator	(777)		×
Select Simulator			
🔿 ModelSim PE			
● ModelSim SE 🔶 选择Moselsim			
O ModelSim DE			
🔿 Questa Simulator			
O Riviera-PRO			
O Active-HDL			
Select 32-Bit or 64-Bit Format			
● 32-Bit 根据实际安装情况,选择是32位还是64位的ModelSim			
0 64-Bit			
Simulator Executable Location (The -p command-line option)			
C: \modeltech_10.0o \win32 选择ModelSim实际安装目录		Browse	
Compxlib Configuration File (The -ofg command-line option)			
compxlib. cfg		Browse	
Compxlib Log File (The -log command-line option)			
compulib.log		Browse	
Do not use this wizard For ISim or ModelSim Xilinx Editiion as they come with pre-compiled simulation libraries. Only specific versions of t supported Please verify that the selected simulator version satisfies the following requirements: ModelSim/Questa Simulator 10.1a and later Riviera 2010.10 or later Active-HDL 8.3 or later	the simula	tors are	

选择语言,选择 Both VHDL and Verilog,点击 next。

Nilinx Simulation Library Compilation Wizard - Indicate the HDLs supported by your simulator	beam			X
Select HDL(s) used for simulation				
● Both VMDL and Verilog → 选择 DOTH VHDL and Verilog				
O VHDL				
O Verilog				
Please ensure that simulator is licensed for selected $HDL(s)$.				
After compilation, the following types of simulations: can be performed				
- Behavioral Simulation in VHDL and Verilog				
- Structural Simulation in VHDL and Verilog - Timing Simulation in VHDL and Verilog				
More Info	< Back	Next >	Can	.cel
个做修改,选择全部器件,点击 next。				

Nilinx Simulation Library Compilation Wizard - Select Device Families		_8		Х
Select Device Familes				
🗹 All FFGA Device Families				
All CPLD Device Families				
<pre>V Artix7 Artix7 Low Voltage Antomotive 9500XL Automotive CoolRunner2 Automotive CoolRunner2 Automotive Spartan3A Automotive Spartan3A Automotive Spartan3A Automotive Spartan3A Automotive Spartan3B Automotive Spartan3B Automotive Spartan3B Automotive Zynq CoolRunner2 CPLDs CoolRunner2 CPLDs CoolRunner2 CPLDs Defense-Grade Kintex7 Defense-Grade Kintex7 Defense-Grade Kintex7 Defense-Grade Kintex7 Defense-Grade Kintex7 Defense-Grade Virtex-6Q Defense-Grade Virtex-6Q Defense-Grade Virtex-6Q Defense-Grade Virtex-6Q Defense-Grade Virtex-6Q Defense-Grade Virtex-7 Defense-Grade Virtex-7 Mintex7 Kintex7 Kintex7 Kintex7 Space-Grade Virtex-4QV Spartan3 Snartan3A and Snartan3AM CoolRunner2 CoolRu</pre>				
More Info	< Back Nex	ıt >	Cano	el

More into 直接点击 next。

and Xilinx Simulation Library Compilation Wizard - Select Simulation Libraries		()		×
Select libraries for Functional and Timing Simulation				
🖂 All libraries				
PFGA designs(UNISDM)				
CPLD designs (COOLRUNNER UN19000)				
CORE Generator (XilinxCoreLib)				
I Timing Simulation library for FPGA and CPLD designs (SIMPRIM)				
🖂 EDK Simulation Library				
Specify more library source path (The -source_lib command-line option):				
More Info	< Back Next	>	Canc	el

根据安装实际情况,指定输出仿真库文件目录到EDK文件夹下,G:\Xilinx\14.7\ISE_DS\EDK,然后点击launch compile process 自动生成仿真库

Nilinx Simulation Library Compilation Wizard - Output directory for compiled libraries —	□ ×
Output directory for compiled libraries	
G:\Xilinx\14.7\ISE_DS\EDK	Browse
	Defen]+
	Deladit
Map only to existing pre-compiled libraries (i. e. no ¬w overwrite command-line option) ✓ Exclude superseded (-exclude_superseded option for EDK only) □ Exclude sublib (-exclude_sublib option for EDK only)	
Advanced options	
You need to remove those entries in angle brackets if you are changing the location to something other than the default.	
Choosing Map only option is same as not including —w argument in compxlib	
More Info Sack Launch Compile Process >	Cancel

Niinx Simulation Library Compilation Wizard - Start Compilation				ß
Compiling Simulation Libraries				
0%				0
0% / /// / VENDOR : Xilinx Inc. / // / VERSION : 14.7 (P.20131013) \ APPLICATION : compxlib / / APPLICATION : compxlib / / CONTENTS : Compilation Log / // / FILENAME : compxlib.log / // / FILENAME : compxlib.log / /// / VILIANAME : compxlib.log / /// /// VILIANAME : compxlib.log / // // / VILIANAME : compxlib.log / // // // VILIANAME : compxlib.log / // // / VILIANAME : compxlib.log / // // // VILIANAME : compilation Mode = FAST Execute Mode = ON Scheduling library installation & compilation for architectures: all Signature:- VILIANAME : compilation for libraries: all Signature:- VILIANAME : compilation /// // // // // /////////////////////				•
<			>	¥
Lore Info	< Back	Next >	Cance	el

🖄 Xilinx Simulation Library Compilation Wizard - Compilation Summary



Compilation Summary

Library	Lang	Mapped Name(s)	Err#(s)	Warn#(s)
secureip	verilog	secureip	0	0
misim	vhdl	unisim	0	1
misim	verilog	unisims_ver	0	0
imprim	vhdl	simprim	0	1
imprim	verilog	simprims_ver	0	0
ilinxcorelib	vhdl	xilinxcorelib	0	357
ilinxcorelib	verilog	xilinxcorelib_ver	0	1
ni9000	verilog	uni9000_ver	0	0
oolrunner	vhdl	cpld	0	0
			100	
coolrunner	verilog	opld_ver	0	0
zoolrunner	verilog	opld_ver		U

点击"Finish",完成Xilinx 仿真库的编译,直接去输出仿真库的路径下可以 找到 modelsim.ini 文件。

i modelsim.ini	2017/11/22 18:08	配置设置	86 KB
ileset.txt	2017/11/15 16:23	文本文档	1 KB
💿 .cxl.mti_se.nt.cmd	2017/11/22 18:08	Windows 命令脚本	94 KB
.compedklib_ise_info	2017/11/22 17:46	COMPEDKLIB_IS	1 KB
📙 xilinxcorelib_ver	2017/11/22 17:45	文件夹	
xilinxcorelib	2017/11/22 17:44	文件夹	
📙 unisims_ver	2017/11/22 17:27	文件夹	
📙 unisim	2017/11/22 17:24	文件夹	
📙 unimacro_ver	2017/11/22 17:27	文件夹	
unimacro	2017/11/22 17:23	文件夹	
📙 uni9000_ver	2017/11/22 17:46	文件夹	
hird_party	2017/11/15 16:07	文件夹	
sw	2017/11/15 15:59	文件夹	
🦲 simprims_ver	2017/11/22 17:33	文件夹	
📙 simprim	2017/11/22 17:31	文件夹	
📙 secureip	2017/11/22 17:19	文件夹	
📙 msg	2017/11/15 16:00	文件夹	
lib	2017/11/15 16:00	文件夹	
hw	2017/11/15 16:00	文件夹	
gnuwin	2017/11/15 16:20	文件夹	
gnu	2017/11/15 15:59	文件夹	
edk	2017/11/22 18:08	文件夹	
eclipse	2017/11/15 15:59	文件夹	
doc	2017/11/15 15:59	文件夹	
data	2017/11/15 16:22	文件夹	
cpld ver	2017/11/22 17:46	文件夹	
cpld	2017/11/22 17:46	文件夹	
board	2017/11/15 16:00	文件夹	
bin	2017/11/15 16:09	文件夹	
xinstall	2017/11/15 16:23	文件夹	

使用记事本或其他文本编辑器打开 modelsim. ini 文件, 先找到这个 library 项。



接着往后看,找到这段代码,这是 modelsim 仿真库的配置路径,复制这段代码

47 secureip = G:\Xilinx\14.7\ISE_DS\EDK/secureip 48 unisim = G:\Xilinx\14.7\ISE_DS\EDK/unisim 49 unimacro = G:\Xilinx\14.7\ISE_DS\EDK/unimacro 50 unisims_ver = G:\Xilinx\14.7\ISE_DS\EDK/unimacro_ver 51 unimacro_ver = G:\Xilinx\14.7\ISE_DS\EDK/unimacro_ver 52 simprim = G:\Xilinx\14.7\ISE_DS\EDK/simprim 53 simprims_ver = G:\Xilinx\14.7\ISE_DS\EDK/simprims_ver 54 xilinxcorelib = G:\Xilinx\14.7\ISE_DS\EDK/xilinxcorelib 55 xilinxcorelib_ver = G:\Xilinx\14.7\ISE_DS\EDK/xilinxcorelib_ver 56 uni9000_ver = G:\Xilinx\14.7\ISE_DS\EDK/uni9000_ver 57 cpld = G:\Xilinx\14.7\ISE_DS\EDK/cpld 58 cpld_ver = G:\Xilinx\14.7\ISE_DS\EDK/cpld_ver 59 edk = G:\Xilinx\14.7\ISE_DS\EDK/edk

Χ,

去到 modelsim 安装路径下,找到 modelsim. ini 文件。

	ieeepure	2017/10/12 12:29	文件夹	
	include	2017/10/12 12:29	文件夹	
	mc2_lib	2017/10/12 12:29	文件夹	
	modelsim_lib	2017/10/12 12:29	文件夹	
	ovm-2.0.3	2017/10/12 12:29	文件夹	
	ovm-2.1.1	2017/10/12 12:29	文件夹	
	ovm-2.1.2	2017/10/12 12:29	文件夹	
	pa_lib	2017/10/12 12:29	文件夹	
	perl_src	2017/10/12 12:29	文件夹	
	std	2017/10/12 12:29	文件夹	
	std_developerskit	2017/10/12 12:29	文件夹	
	sv_std	2017/10/12 12:29	文件夹	
	synopsys	2017/10/12 12:29	文件夹	
	tcl	2017/10/12 12:29	文件夹	
	upf_lib	2017/10/12 12:29	文件夹	
	upf_src	2017/10/12 12:29	文件夹	
	uvm_reg-1.1	2017/10/12 12:29	文件夹	
	uvm-1.0-EA	2017/10/12 12:29	文件夹	
	uvm-1.0p1	2017/10/12 12:29	文件夹	
	uvm-1.1	2017/10/12 12:29	文件夹	
	verilog	2017/10/12 12:29	文件夹	
	verilog_src	2017/10/12 12:28	文件夹	
	vhdl_src	2017/10/12 12:28	文件夹	
	vital2.2b	2017/10/12 12:29	文件夹	
	vital1995	2017/10/12 12:29	文件夹	
	vital2000	2017/10/12 12:29	文件夹	
	vm_src	2017/10/12 12:29	文件夹	
	win32	2017/10/12 13:48	文件夹	
].default_vopt_flow_on	2011/7/22 14:02	DEFAULT_VOPT	1 KE
	LICENSE	2011/7/22 14:02	文件	27 KE
	LICENSE.TXT	2017/10/12 13:49	文本文档	465 KE
2] modelsim.ini	2017/11/28 17:25	配置设置	71 KE
] modelsim.ini~	2011/7/22 14:02	INI~ 文件	69 KE
Ľ	RELEASE_NOTES	2011/7/22 17:37	文件	62 KE
	RELEASE_NOTES.html	2011/7/22 17:37	360 Chrome HT	62 KE
	RELEASE_NOTES.txt	2011/7/22 17:37	文本文档	63 KE
] vco	2011/7/22 14:02	文件	8 KE

使用记事本或其他文本编辑器打开 modelsim. ini 文件,找到其中的 library 项。



打开 ISE 软件, 进行 modelsim 连接配置

打开 edit-》 preference -》 integrated tools, model tech simulator 选择 modelsim.exe 所在路径。

Category Set the paths for the integrated tools you have installed. Image: Console Model Tech Simulator: Image: Star Editors C: \modeltech_10.0c/win32\modelsim.exe Image: Star Editor Symplify: Image: Star Editor Default Symplify: Default Precess Completi Default Precision: Default Color Scheme Default Precision: Default Colors Default Device Families Default Wath "design properties" Mathead:	Preferences - Integrated	Tools Options	×
Console Model Teoh. Simulator: HTML Browser Design Goals & S Design Goals & S Symplify: Process Completi Symplify Pro: SS Text Editor Default New Object Color Object Color Object Colors Default PlanAbeed: Default Prevision: Default Parableed: Default OK Cancel Apply Help	Category	Set the paths for the integrated tools you have ins	stalled.
INL Browser ISE General Design Goals & S Editors Integrated Tools Process Completi Symplify Pro: ISE Text Editor Language Templates RTL/Technology View Color Scheme New Object Color Ubject Color Ubject Color Object Colors Device Families Layout Xth "design properties"	Console	Model Tech Simulator:	
Design Goals & S Symplify: #### Integrated Tools Default Process Completi Default Symplify Pro: Default Symplify Pro: Default Symplify Colors Default Precision: Default Color Scheme Default New Object Color Object Color User Color Rules G: \Kilinx\14.7\ISE_DS\FlamAhead\bin Default Default	- ISE General	C:\modeltech_10.Oc\win32\modelsim.exe	选择Modelsim的安
Editors Integrated Tools Process Completi Symplify Pro: Symplify Pro: Symplify Pro: Symplify Pro: Symplify Pro: Symplify Pro: Prevision: Color Scheme New Object Color User Color Rules Schematic Editor Check Colors Device Families Layout Wath "design properties" OK Cancel Apply Help	- Design Goals & S	Symplify:	装路径
Process Complet ISE Text Editor Language Templates RTL/Technology View Color Scheme New Object Color Object Color User Color Rules Schematic Editor Check Colors Device Families Layout K击 "design properties" Stat "design properties"	- Editors		Default
ISE Text Editor Language Templates RTL/Technology View New Object Color Object Colors User Color Rules Schematic Editor Check Colors Device Families Layout 文 K击 "design properties"	Process Completi	Symplify Pro:	
Language lemplates Precision: Color Scheme Default New Object Color Object Color User Color Rules G:\Xilinx\14.7\ISE_DS\Flankhead\bin Schematic Editor Default Check Colors Device Families Default Layout *	ISE Text Editor		Default
Color Scheme Default New Object Color Object Colors Object Color Rules G: Xilinx\14.7\ISE_DS\PlanAhead\bin Schematic Editor Default Check Default OK Cancel Apply Help	Language Templates	Precision:	
New Object Color Object Colors User Color Rules Schematic Editor Check Colors Device Families Layout 文 包括 "design properties"	Color Scheme		Default
User Color Rules User Color Rules Schematic Editor Check Colors Device Families Layout X击 "design properties"	New Object Color	PlanAhead:	
Schematic Editor Check Colors Layout 文 低于"design properties"	User Color Rules	G:\Xilinx\14.7\ISE_DS\PlanAhead\bin	. Default
Check Colors Device Families Layout 东击"design properties"	Schematic Editor	n na se a reserva na konferencia da la serva na serva na nasko na serva na serva na serva na serva na serva na	
Colors Device Families Layout 武击"design properties"	- Check		
Device Families Layout 文 武士"design properties"	Colors		
Layout 、 OK Cancel Apply Help 东击"design properties"	Device Families		
OK Cancel Apply Help 法击"design properties"	Layout		
OK Cancel Apply Help 気击"design properties"			
东击"design properties"		OK Car	ncel Apply Help
法击"design properties"			
	点击"design prope	erties"	
		7 1 1	
A A A A A A A A A A A A A A A A A A A			
		Y	
XI			
4			



simulator 选择 modelsim-SE Verilog

≽ Design Properties		×
Name:	fft_pro	
Location:	C:\Users\irene\Desktop\ceshi11\fft_pro	
Working directory:	C:\Users\irene\Desktop\ceshi11\fft_pro	
Description:		
Project Settings		
Property Name	Value	
Top-Level Source Type	HDL	~
Evaluation Development Board	None Specified	
Product Category	All	v
Family	Spartan6	~
Device	XC6SLX4	~
Package	TQG144	~
Speed	-3	~
Synthesis Tool	XST (VHDL/Verilog)	~
Simulator	Modelsim-SE Verilog	~
Preferred Language	Verilog	~
Property Specification in Project File	Store all values	~
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	~
Enable Message Filtering		
	OK Cancel Hely	p

点击"OK",至此,Xilinx 仿真库编译完毕。